DOCKET NO. 98-MET-069C1 (STMI01-01012)
Customer No. 30425

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of	:	David L. Isaman
U.S. Serial No.	:	09/443,160
Filed	:	November 19, 1999
For	:	SYMBOLIC STORE-LOAD BYPASS
Group No.	:	2183
Examiner	:	Daniel H. Pan

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

The undersigned hereby certifies that the following documents:

1. Appeal Brief;
2. Check in the amount of $340.00 for the Appeal Brief filing fee;
3. Fee Transmittal for FY 2005 (in duplicate); and
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Date: December 6, 2004

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Date: Dec. 6 2004

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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 340.00

Complete if Known	
Application Number	09/443,160
Filing Date	November 19, 1999
First Named Inventor	David L. Isaman
Examiner Name	Daniel H. Pan
Art Unit	2183
Attorney Docket No.	98-MET-069C1 (STMI01-01012)

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 50-0208

Deposit Account Name: Davis Munck, P.C.

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

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FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) -0-

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) -0-

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	$340.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 340.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	William A. Munck	*Registration No. (Attorney/Agent)*	39,308	*Telephone*	972-628-3600
Signature				*Date*	December 6, 2004

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DOCKET NO. 98-MET-069C1 **PATENT**
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Sir:

APPEAL BRIEF

The Appellant has appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated June 1, 2004, finally rejecting Claims 2-5 and 12-15. The Appellant filed a Notice of Appeal on September 29, 2004, which was received on October 4, 2004. The Appellant respectfully submits this brief on appeal with the statutory fee of $340.00.

REAL PARTY IN INTEREST

This application is currently owned by STMicroelectronics, Inc. as indicated by:

(1) an assignment recorded on January 24, 2000 in the Assignment Records of the United States Patent and Trademark Office at Reel 010517, Frame 0988; and

(2) a merger recorded on August 2, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 012036, Frame 0306.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claim 1 has been cancelled. Claims 2-5 and 12-15 have been rejected pursuant to a final Office Action dated June 1, 2004. Claims 6-11 and 16-19 have been objected to as being allowable but depending from rejected base claims pursuant to the final Office Action dated June 1, 2004. Claims 20 and 21 have been allowed pursuant to the final Office Action dated June 1, 2004. Claims 2-5 and 12-15 are presented for appeal. A copy of all pending claims is provided in Appendix A.

STATUS OF AMENDMENTS

The Appellant filed an AMENDMENT AND RESPONSE UNDER 37 C.F.R. § 1.116 on August 2, 2004. The Examiner refused to enter the AMENDMENT AND RESPONSE, asserting that it did not place

the application in better form for appeal by materially reducing or simplifying the issues for appeal.

SUMMARY OF CLAIMED SUBJECT MATTER

Regarding Claim 2, a pipelined microprocessor 100 is capable of detecting an instruction 151 that loads data from a first memory location that was previously stored to. (*Application, Page 8, Line 6 – Page 9, Line 7; Page 11, Line 8 – Page 12, Line 11*). The instruction 151 is detected without requiring computation of an external memory address of the first memory location for the instruction 151. (*Application, Page 9, Lines 9-11*).

Regarding Claim 12, a method for operating a pipelined microprocessor 100 includes detecting in the pipelined microprocessor 100 an instruction 151 that loads data from a first memory location that was previously stored to. (*Application, Page 8, Line 6 – Page 9, Line 7; Page 11, Line 8 – Page 12, Line 11*). The instruction 151 is detected without requiring computation of an external memory address of the first memory location for the instruction 151. (*Application, Page 9, Lines 9-11*).

GROUNDS OF REJECTION

1. Claims 2-5 and 12-15 stand rejected under 35 U.S.C. § 102(a) or § 102(b) as being anticipated by U.S. Patent No. 5,475,823.

2. Claims 2-5 and 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,475,823 in view of U.S. Patent No. 6,360,314.

ARGUMENT

I. GROUND OF REJECTION #1 (§ 102 REJECTION)

The rejection of Claims 2-5 and 12-15 under 35 U.S.C. § 102(a) or § 102(b) is improper and should be withdrawn.

A. OVERVIEW

Claims 2-5 and 12-15 stand rejected under 35 U.S.C. § 102(a) or § 102(b) as being anticipated by U.S. Patent No. 5,475,823 to Amerson et al. ("*Amerson*").

A copy of *Amerson* is provided in Appendix B.

B. STANDARD

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. (*MPEP § 2131; In re Bond, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990)*). Anticipation is only shown where each and every limitation of the claimed invention is found in a single prior art reference. (*MPEP § 2131; In re Donohue, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985)*).

C. THE *AMERSON* REFERENCE

Amerson recites a memory processor that prevents errors when a compiler advances load instructions in a sequence of instructions. (*Abstract*). The processor intercepts all load and store

instructions before the instructions enter a memory pipeline. (*Abstract*). The processor stores a load instruction for a particular period of time, which allows the processor to determine if a store instruction to the same address would have been executed before the load instruction. (*Abstract*). If a store instruction would have been executed, the processor uses the data from the store instruction for the load instruction. (*Abstract*). As part of the processor's operation, an address comparator 28 compares the memory address specified in a store instruction with memory addresses specified in load instructions. (*Col. 5, Lines 30-33*). In other embodiments, an address comparator 528 compares memory addresses from all store instructions to the memory addresses from load instructions to "check for partial or complete overlap of the memory locations accessed by the load and store instructions." (*Col. 8, Lines 28-33*).

D. CLAIMS 2-5 AND 12-15

Claim 2 recites:

> [a] pipelined microprocessor capable of detecting an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

The Examiner fails to establish that *Amerson* anticipates all elements of Claim 2. In particular, the Examiner fails to establish that *Amerson* anticipates a microprocessor capable of detecting an instruction "without requiring computation of an external memory address of [a] first memory location for the instruction."

In every embodiment of *Amerson*, the processor compares the actual memory addresses being

accessed by load and store instructions. More specifically, the address comparator in *Amerson* compares the memory addresses being accessed by load and store instructions. It is clear here that *Amerson* operates by requiring computation of external memory addresses. The external memory addresses for load and store instructions must be computed before the address comparator of *Amerson* can compare memory the addresses. As a result, *Amerson* fails to anticipate detecting an instruction that loads data from a "first memory location ... without requiring computation of an external memory address of [the] first memory location for the instruction" as recited in Claim 2.

In order to reject Claim 2 as being anticipated by *Amerson*, the Examiner attempts to distinguish between address computation and instruction detection (using address comparison) in *Amerson*. The Examiner asserts that detecting instructions involves comparing addresses, not computing addresses. (*See, e.g., 06/01/04 Office Action, Page 5, Paragraph 16*). This enables the Examiner to assert that the phrase "without requiring computation of an external memory address" in Claim 2 does not "necessarily exclude the requirement of a computation of external address before the detection of the instruction." (*09/07/04 Advisory Action, Page 2, First paragraph*).

This position is completely illogical. This position basically asserts that the phrase "without requiring computation of an external memory address" can be interpreted as "requiring computation of an external memory address." This is not a proper interpretation of Claim 2. Claim 2 is perfectly clear – an instruction that loads data from a first memory location is detected "without requiring computation of an external memory address of [the] first memory location for the instruction."

Amerson must compute the memory addresses for load and store instructions before the address comparator can compare those memory addresses. As a result, *Amerson* clearly does not

anticipate detecting an instruction that loads data from a first memory location "without requiring computation of an external memory address of [the] first memory location for the instruction" as recited in Claim 2.

For these reasons, *Amerson* fails to anticipate the Appellant's invention as recited in Claim 2 (and its dependent claims). For similar reasons, *Amerson* fails to anticipate the Appellant's invention as recited in Claim 12 (and its dependent claims).

Accordingly, the Appellant respectfully requests that the § 102 rejection of Claims 2-5 and 12-15 be withdrawn and that Claims 2-5 and 12-15 be passed to allowance.

II. GROUND OF REJECTION #2 (§ 103 REJECTION)

The rejection of Claims 2-5 and 12-15 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 2-5 and 12-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over *Amerson* in view of U.S. Patent No. 6,360,314 to Webb, Jr. et al. ("*Webb*").

A copy of *Webb* is provided in Appendix C.

B. STANDARD

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262,*

23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (*MPEP § 2142*).

C. THE *WEBB* REFERENCE

Webb recites a bypass mechanism for a computer system. (*Abstract*). The bypass mechanism includes a store queue 426 and a store data buffer 428. (*Col. 5, Lines 49-54*). The store queue 426 contains information about store instructions that have not been completed, such as the physical memory address associated with a store instruction. (*Col. 5, Lines 58-60*). The store data buffer 428 stores the actual data values to be written to memory by the store instructions contained in the store queue 426. (*Col. 5, Lines 53-54*). The bypass mechanism compares the address from a load instruction to the addresses from the store instructions in the store queue 426. (*Col. 6, Lines 6-10*). If a match is found in the store queue 426, the bypass mechanism uses data from the store data buffer 428 to satisfy the load instruction. (*Col. 6, Lines 10-12*).

D. CLAIMS 2-5 AND 12-15

Claim 2 recites:

> [a] pipelined microprocessor capable of detecting an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

The Examiner fails to establish that the proposed *Amerson-Webb* combination discloses, teaches, or suggests all elements of Claim 2. In particular, the Examiner fails to establish that the proposed *Amerson-Webb* combination discloses, teaches, or suggests a microprocessor capable of detecting an instruction "without requiring computation of an external memory address of [a] first memory location for the instruction."

As shown above, *Amerson* requires computation of external memory addresses for load and store instructions in order to operate. *Webb* also requires computation of external memory addresses for load and store instructions in order to operate.

Webb specifically recites that the bypass mechanism compares the physical address of a load instruction to the physical addresses of store instructions by comparing "bits 43:13" of the physical addresses. (*Col. 6, Lines 6-10*). It is clear here that *Webb* must compute the physical addresses of load and store instructions in order to identify load and store instructions that refer to the same external memory address. As a result, *Webb* fails to anticipate detecting an instruction that loads data from a "first memory location ... without requiring computation of an external memory address of [the] first memory location for the instruction" as recited in Claim 2.

The Examiner asserts that the system of *Webb* is used to avoid unnecessary retrievals from external memory and that if a "retrieval from the memory was avoided, the actual effective address of the memory must not have been calculated." (*06/01/04 Office Action, Page 6, Paragraph 17*). Basically, the Examiner argues that if an external memory was not accessed, the physical memory address for a memory location must not have been calculated.

This argument by the Examiner assumes that an external memory address is never calculated if the external memory is not accessed. This assertion in contradicted by the express recitations in *Webb*. *Webb* specifically recites that "bits 43:13" of the physical address are used by the system of *Webb*. (*Col. 6, Lines 3-10*). Using these bits of the physical address, a fetch to external memory may or may not occur. (*Col. 6, Lines 10-17*).

Both *Amerson* and *Webb* must compute memory addresses for load and store instructions in

order to operate. As a result, the proposed *Amerson-Webb* combination clearly does not disclose, teach, or suggest detecting an instruction that loads data from a first memory location "without requiring computation of an external memory address of [the] first memory location for the instruction" as recited in Claim 2.

For these reasons, the proposed *Amerson-Webb* combination fails to disclose, teach, or suggest the Appellant's invention as recited in Claim 2 (and its dependent claims). For similar reasons, the proposed *Amerson-Webb* combination fails to disclose, teach, or suggest the Appellant's invention as recited in Claim 12 (and its dependent claims).

Accordingly, the Appellant respectfully requests that the § 103 rejection of Claims 2-5 and 12-15 be withdrawn and that Claims 2-5 and 12-15 be passed to allowance.

SUMMARY

The Appellant has demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellant respectfully requests the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellant has enclosed the appropriate fee to cover the cost of this APPEAL BRIEF. The Appellant does not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) or credit any overpayments to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Dec. 6, 2004

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APPENDIX A

PENDING CLAIMS

1. (Cancelled).

2. A pipelined microprocessor capable of detecting an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

3. A pipelined microprocessor as claimed in Claim 2 wherein said pipelined microprocessor is capable of detecting an instruction that stores data into a second memory location that was previously read from without computing an external memory address of said second memory location.

4. A pipelined microprocessor as claimed in Claim 2 wherein said pipelined microprocessor is capable of detecting instructions that load data from identical memory locations that were previously stored to without computing external memory addresses of said identical memory locations.

5. A pipelined microprocessor as claimed in Claim 3 wherein said pipelined microprocessor is capable of detecting instructions that store data into identical memory locations that were previously read from without computing external memory addresses of said identical memory locations.

6. A pipelined microprocessor as claimed in Claim 4 wherein said pipelined microprocessor is capable of examining symbolic structure of said instructions that load data from identical memory locations that were previously stored to, and capable of detecting said instructions that load data from identical memory locations by examining said symbolic structure.

7. A pipelined microprocessor as claimed in Claim 5 wherein said pipelined microprocessor is capable of examining symbolic structure of said instructions that store data into identical memory locations that were previously read from, and capable of detecting said instructions that store data into identical memory locations by examining said symbolic structure.

8. A pipelined microprocessor as claimed in Claim 6 wherein said pipelined microprocessor is capable of detecting said instructions that load data from identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor.

9. A pipelined microprocessor as claimed in Claim 7 wherein said pipelined microprocessor is capable of detecting said instructions that store data into identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor.

10. A pipelined microprocessor as claimed in Claim 6 wherein said pipelined microprocessor comprises:

an instruction decode stage capable of detecting said instructions that load data from identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor; and

a bypass element capable of sending a bypass signal to an instruction execution stage of said pipelined microprocessor that indicates that said instructions refer to an identical memory location.

11. A pipelined microprocessor as claimed in Claim 7 wherein said pipelined microprocessor comprises:

an instruction decode stage capable of detecting said instructions that store data into identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor; and

a bypass element capable of sending a bypass signal to an instruction execution stage of said pipelined microprocessor that indicates that said instructions refer to an identical memory location.

12. A method for operating a pipelined microprocessor, said method comprising:

detecting in said pipelined microprocessor an instruction that loads data from a first memory location that was previously stored to, wherein the instruction is detected without requiring computation of an external memory address of said first memory location for the instruction.

13. A method for operating a pipelined microprocessor as claimed in Claim 12, said method further comprising:

detecting in said pipelined microprocessor an instruction that stores data into a second memory location that was previously read from without computing an external memory address of said second memory location.

14. A method for operating a pipelined microprocessor as claimed in Claim 12, said method further comprising:

detecting in said pipelined microprocessor instructions that load data from identical memory locations that were previously stored to without computing external memory addresses of said identical memory locations.

15. A method for operating a pipelined microprocessor as claimed in Claim 13, said method further comprising:

detecting in said pipelined microprocessor instructions that store data into identical memory locations that were previously read from without computing external memory addresses of said identical memory locations.

16. A method for operating a pipelined microprocessor as claimed in Claim 14, said method further comprising:

examining in said pipelined microprocessor symbolic structure of said instructions that load data from identical memory locations that were previously stored to; and

detecting said instructions that load data from identical memory locations by examining said symbolic structure.

17. A method for operating a pipelined microprocessor as claimed in Claim 15, said method further comprising:

examining in said pipelined microprocessor symbolic structure of said instructions that store data into identical memory locations that were previously read from; and

detecting said instructions that store data into identical memory locations by examining said symbolic structure.

18. A method for operating a pipelined microprocessor as claimed in Claim 16, said method further comprising:

detecting in an instruction decode stage of said pipelined microprocessor said instructions that load data from identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor; and

sending a bypass signal from a bypass element to an instruction execution stage of said pipelined microprocessor wherein said bypass signal indicates that said instructions refer to an identical memory location.

19. A method for operating a pipelined microprocessor as claimed in Claim 17, said method further comprising:

detecting in an instruction decode stage of said pipelined microprocessor said instructions that store data into identical memory locations by identifying an identical offset address value from an identical base address value in a register within said pipelined microprocessor; and

sending a bypass signal from a bypass element to an instruction execution stage of said pipelined microprocessor wherein said bypass signal indicates that said instructions refer to an identical memory location.

20. A method for operating a pipelined microprocessor, said method comprising:

detecting a first instruction that stores data to a first memory location, said first instruction comprising syntax for computing an effective address for said first memory location;

detecting a second instruction that loads data from a second memory location, said second instruction comprising syntax for computing an effective address for said second memory location;

determining said syntax for said first instruction and said syntax for said second instruction;

using said syntax for said first instruction and said syntax for said second instruction to determine a relationship between said first memory location and said second memory location, without computing said effective address for said first memory location and without computing said effective address for said second memory location; and

using said relationship to determine whether to perform one of said first instruction and said second instruction.

21. A method for operating a pipelined microprocessor as claimed in Claim 20 wherein said syntax for said first instruction and said syntax for said second instruction refer to an identical memory location.

APPENDIX B

***Amerson* Reference**

U.S. Patent No. 5,475,823

APPENDIX C

***Webb* Reference**

U.S. Patent No. 6,360,314